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Koji Hirairi

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EXAMINER

TANG, KENNETH

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/801,308	Applicant(s) HIRAIRI, KOJI	
	Examiner KENNETH TANG	Art Unit 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 February 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>2/16/10</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1- 39 are presented for examination.
2. This action is in response to the Amendment/Remarks on 4/16/10. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 4 of copending Application No. 10/849623, as most recently amended.
4. Similarly, claims 10 and 25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 55 of copending Application No. 10/849623, as most recently amended.

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5. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of claim 4 (which depends on claim 3, which depends on claim 1) contains, and thus anticipates, the limitations of claim 1 of the Instant Application. Similarly, the limitations of claims 10 and 25 contain, and thus anticipates, the limitations of claim 55. A table has been constructed below to illustrate this (emphasis by Examiner):

INSTANT APPLICATION	APPLICATION 10/849623 <i>(as most recently amended)</i>
<p>1. A method, comprising:</p> <p>monitoring processor tasks and associated processor loads therefor that are allocated to be performed by respective sub-processing units associated with a main processing unit;</p> <p>re-allocating at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and</p>	<p>1. A method, comprising:</p> <p>monitoring processor tasks and associated processor loads therefor that are allocated to be performed by respective participating sub-processing units associated with a main processing unit;</p> <p>detecting whether a processing error has occurred in a given one of the sub-processing units;</p> <p>re-allocating all of the processor tasks of the given sub-processing unit to one or more of the participating sub-processing units based on the processor loads of the processor tasks of the given sub-processing</p>

<p>in response to the reallocation, commanding the sub-processing units that are not scheduled to perform any tasks because of the reallocation into a low power consumption state.</p>	<p>unit and the processor loads of the participating sub-processing units; and performing at least one of (i) shutting down; and (ii) re-booting the given sub-processing unit.</p> <p>3. The method of claim 1, further comprising: assigning the processor tasks among the sub-processing units such that at least one of the sub-processing units is substantially unloaded and available to receive some or all of the processor tasks from the given sub-processing unit.</p> <p>4. The method of claim 3, further comprising commanding the at least one substantially unloaded sub-processing unit that is not scheduled to perform any processor tasks into a stand-by state.</p>
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<p>10. An apparatus, comprising:</p> <p>a plurality of sub-processing units, each operable to perform processor tasks; and</p> <p>a main processing unit operable to:</p> <p>(i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units;</p> <p>(ii) re-allocate at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and</p> <p>(iii) in response to the reallocation, issue a power-off command indicating that the sub-processing units that are not</p>	<p>49. An apparatus, comprising:</p> <p>a plurality of participating sub-processing units, each operable to perform processor tasks; and</p> <p>a main processing unit operable to:</p> <p>(i) monitor the processing tasks and associated processor loads therefor that are allocated to be performed by the respective participating sub-processing units;</p> <p>(ii) detect whether a processing error has occurred in a given one of the sub-processing units;</p> <p>(iii) re-allocate all of the processor tasks of the given sub-processing unit to one or more of the participating sub-processing units based on the processor loads of the processor tasks of the given sub-processing unit and the processor loads of the participating sub-processing units; and</p> <p>(iv) at least one of issue a shut-down command and issue a re-boot command to the given sub-processing unit.</p>
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<p>scheduled to perform any tasks should enter a low power consumption state.</p>	<p>54. The apparatus of claim 49, wherein the main processing unit is further operable to assign the processor tasks among the sub-processing units such that at least one of the sub-processing units is substantially unloaded and available to receive some or all of the processor tasks from the given sub-processing unit.</p> <p>55. The apparatus of claim 54, wherein the main processing unit is further operable to command the one or more unloaded sub-processing units that are not scheduled to perform any processor tasks into a stand-by state.</p>
<p>25. A main processor operating under the control of a software program to perform steps, comprising:</p> <p>monitoring processor tasks and</p>	<p>49. An apparatus, comprising:</p> <p>a plurality of participating sub-processing units, each operable to perform processor tasks; and</p> <p>a main processing unit operable to:</p> <p>(i) monitor the processing tasks and</p>

<p>associated processor loads therefor that are allocated to be performed by respective sub-processing units associated with the main processing unit;</p> <p>re-allocating at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and</p> <p>in response to the reallocation, commanding the sub-processing units that are not scheduled to perform any tasks into a low power consumption state.</p>	<p>associated processor loads therefor that are allocated to be performed by the respective participating sub-processing units;</p> <p>(ii) detect whether a processing error has occurred in a given one of the sub-processing units;</p> <p>(iii) re-allocate all of the processor tasks of the given sub-processing unit to one or more of the participating sub-processing units based on the processor loads of the processor tasks of the given sub-processing unit and the processor loads of the participating sub-processing units; and</p> <p>(iv) at least one of issue a shut-down command and issue a re-boot command to the given sub-processing unit.</p> <p>54. The apparatus of claim 49, wherein the main processing unit is further operable to assign the processor tasks among the sub-processing units such that at least one of the sub-processing units is substantially unloaded</p>
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	<p>and available to receive some or all of the processor tasks from the given sub-processing unit.</p> <p>55. The apparatus of claim 54, wherein the main processing unit is further operable to command the one or more unloaded sub-processing units that are not scheduled to perform any processor tasks into a stand-by state.</p>
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This is a provisional obviousness-type double patenting rejection.

6. Claim 37 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 55 of copending Application No. 10/849623 in view of Matoba (US 5,913,068).

7. The following table has been constructed to illustrate the elements of the Instant Application (bolded) that are disclosed in the claims of Application 10/849623 (bolded), as most recently amended.

INSTANT APPLICATION	APPLICATION 10/849623 <i>(as most recently amended)</i>
<p data-bbox="191 434 792 613">34. An apparatus, comprising: a plurality of sub-processing units, each operable to perform processor tasks; and</p> <p data-bbox="191 798 792 1270"> a bus circularly interconnecting the sub-processing units such that transfers between any two sub-processing units may occur directly as between adjacent sub-processing units or through one or more intermediate sub-processing units as between more distant sub-processing units,</p> <p data-bbox="191 1308 792 1633"> wherein the sub-processing units are operable to: (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units;</p>	<p data-bbox="831 434 1419 686">49. An apparatus, comprising: a plurality of participating sub-processing units, each operable to perform processor tasks; and</p> <p data-bbox="831 724 1419 760"> a main processing unit operable to:</p> <p data-bbox="831 942 1419 1050"><i>(taught in Matoba, see explanation below the table)</i></p> <p data-bbox="831 1381 1419 1633">(i) monitor the processing tasks and associated processor loads therefor that are allocated to be performed by the respective participating sub-processing units;</p> <p data-bbox="831 1671 1419 1850"> (ii) detect whether a processing error has occurred in a given one of the sub-processing units;</p>

(ii) re-allocate at least some of the tasks based on their associated processor loads.	(iii) re-allocate all of the processor tasks of the given sub-processing unit to one or more of the participating sub-processing units based on the processor loads of the processor tasks of the given sub-processing unit and the processor loads of the participating sub-processing units; and
<p>36. The apparatus of claim 34 wherein the re-allocation of the tasks is performed such that at least one of the sub-processing units is not scheduled to perform any tasks.</p>	<p>(iv) at least one of issue a shut-down command and issue a re-boot command to the given sub-processing unit.</p>
<p>37. The apparatus of claim 36, wherein the sub-processing units that are not scheduled to perform any tasks are operable to enter a low power consumption state.</p>	<p>54. The apparatus of claim 49, wherein the main processing unit is further operable to assign the processor tasks among the sub-processing units such that at least one of the sub-processing units is substantially unloaded and available to receive some or all of the processor tasks from the given sub-processing unit.</p>
	<p>55. The apparatus of claim 54, wherein the main processing unit is further operable to</p>

	command the one or more unloaded sub-processing units that are not scheduled to perform any processor tasks into a stand-by state.
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8. As illustrated in the above table, Application No. 10/849623 does not explicitly disclose a bus circularly interconnecting the sub-processing units such that transfers between any two sub-processing units may occur directly as between adjacent sub-processing units or through one or more intermediate sub-processing units as between more distant sub-processing units.

Furthermore, Application No. 10/849623 does not explicitly disclose having the sub-processing units (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and (ii) re-allocate at least some of the tasks based on their associated processor loads. However, Matoba teaches having a plurality of processors (CPU0, CPU1, CPU2, CPU3) (Fig. 1, items 11-14) interconnected by a CPU bus (CPU bus allows for adjacent or intermediate communication), which share access to a “process management table” 23, “load data of each processor” 29, “Process Management Software” 25, “Processor Load Measuring Software” 27, etc., in order to monitor processor tasks and associated processor loads that are allocated to be performed by the respective processors of CPU0, CPU1, CPU2, and CPU3 (see Fig. 1, col. 4, lines 3-6, col. 5, lines 37-39 and 61-63, col. 6, lines 15-19, col. 8, lines 31-42, col. 9, lines 58-67). One of ordinary skill in the art would have known to modify Application No. 10/849623 such that it would include having the sub-

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processing units (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and (ii) re-allocate at least some of the tasks based on their associated processor loads, in addition to a CPU bus that would allow for adjacent or intermediate communication between the sub-processing units, as taught in Matoba's multiprocessing system. The suggestion/motivation for doing so would have been to provide the predicted result of power consumption control that is dynamic, more effectively performed and which allows for finer power consumption control (see Matoba, col. 1, lines 48-57, col. 2, lines 48-52, col. 9, lines 58-65). Therefore, it would have been obvious to one of ordinary skill in the art to combine Application No. 10/849623 and Matoba to obtain the invention of claim 37.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-3, 8-12, 19-20, 22, 24-27, and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (hereinafter Nicol) (US 6,141,762) in view of Buch (US 6,901,522 B2).

10. As to claim 1, Nicol teaches a method, comprising:

monitoring processor tasks and associated processor loads (via OS) (Fig. 2, item 100) therefor that are allocated to be performed by respective sub-processing units (Fig. 2, items 101-104) associated with a main processing unit (Fig. 2, item 100) (col. 5, lines 23-28);

re-allocating at least some of the tasks based on their associated processor loads (col. 2, lines 18-24, col. 3, lines 10-13); and

in response to the re-allocation, commanding the sub-processing units into a low power consumption state (col. 2, lines 25-31).

11. Nicol is silent in having at least one of the sub-processing units not scheduled to perform any tasks because of the reallocation and specifically commanding the sub-processing unit that is not scheduled to perform any tasks into a low power consumption state.

12. However, Buch teaches a multi-processing system that dynamically adjusts processor power based on system workload. Particularly, the method and apparatus determines the minimum number of required processors based on the workload and sets a processor affinity to run on the determined minimum number of required processors. The free/non-required processors enter a low-power state (see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2). Nicol and Buch are analogous art because they are both in the same field of endeavor of multiprocessing and both are attempting to solve the same problem of reducing power consumption. Thus, one of ordinary skill in the art would have known to modify Nicol's

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multiprocessing system and method such that it would include the teachings/concepts of Buch's multiprocessing system, namely, having at least one of the sub-processing units not scheduled to perform any tasks because of the reallocation and specifically commanding the sub-processing unit that is not scheduled to perform any tasks into a low power consumption state. The suggestion/motivation for doing so would have been to provide the predicted result of having the ability to provide CPUs on demand by dynamically bringing more CPU's on-line to meet increased server workload, and vice versa (Buch - col. 4, line 63 through col. 5, lines 1-2). Furthermore, it would optimize efficiency by ensuring that only the minimum number of required processors are being used, while the unused/free processors enter into a low-power state (see Abstract). Therefore, one of ordinary skill in the art would have known to combine the teachings of Nicol and Buch in order to obtain the broadest reasonable interpretation of claim 1.

13. As to claim 2, Nicol teaches wherein: each of the sub-processing units include at least one of: (i) a power supply interrupt circuit (Fig. 2, item 140); and (ii) a clock interrupt circuit (Fig. 2, item 110); and the method includes using at least one of the power supply interrupt circuit and the clock interrupt circuit to place the sub-processing units into the low power consumption state includes in response to the power-off command (col. 4, lines 17-47).

14. As to claim 3, Nicol teaches wherein each of the sub-processing units includes a power supply and the power supply interrupt circuit; and the method includes using the power supply interrupt circuit to shut down the power supply in response to the power-off command to place

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the given sub-processing unit into the low power consumption state (Fig. 2, items 110, 140, col. 4, lines 17-37).

15. As to claim 8, Nicol teaches further comprising reducing the dynamic power dissipation of at least one of the sub-processing units using at least one of the main processing unit and one or more of the sub-processing units to carry out variable clock frequency control (col. 2, lines 11-14, col. 3, lines 24-30).

16. As to claim 9, Nicol teaches further comprising reducing the static and dynamic power dissipation of at least one of the sub-processing units using at least one of the main processing unit and one or more of the sub-processing units to carry out variable power supply (Vdd) control (Fig. 2, item 140, col. 4, lines 17-53).

17. As to claim 10, it is rejected for the same reasons as stated in the rejection of claim 1. Nicol teaches an apparatus that performs the method of claim 1 (see Fig. 2, col. 2, lines 18-31 and 50-64).

18. As to claims 11-12, they are rejected for the same reasons as stated in the rejections of claims 2-3, respectively.

19. As to claims 19-20, they are rejected for the same reasons as stated in the rejections of claims 8-9, respectively.

20. As to claim 22, Nicol teaches wherein the main processing unit 100 is at least one of remotely located from or locally located with one or more of the sub-processing units 101-104 (Fig. 2, items 100, 101, 102, 103, 104).

21. As to claim 24, Nicol (col. 6, lines 34-67) teaches wherein the sub-processing units employ substantially heterogeneous computer architectures or a homogeneous computer architecture.

22. As to claims 25-27 and 32-33, they are rejected for the same reasons as stated in the rejections of claims 1-3 and 8-9, respectively.

23. Claims 4-7, 13-18, and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (hereinafter Nicol) (US 6,141,762) in view of Buch, and further in view of Matoba (US 5,913,068).

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24. As to claim 4, Nicol teaches the main processing unit including an operating system (OS) that dynamically allocates the tasks based on processor load (see Abstract). However, Nicol in view of Buch is silent in explicitly teaching a task load table containing the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and the method includes using the main processing unit to update the task load table in response to any changes in tasks and loads. Matoba teaches a main processor (CPU 18) dynamically distributing processes to a plurality of sub-processors (CPUs 11-14) based on a process management table 23 and process management software 27 such that performance and power consumption is improved (Fig. 1, items 11-14, 18, 23, 25, 27, 29, col. 3, lines 30-43, col. 4, lines 3-6, col. 9, lines 58-65). Nicol, Buch and Matoba are all analogous art because they are in the same field of endeavor of multiprocessing and all attempting to solve the same problem of improving power management/conservation. One of ordinary skill in the art would have known to modify Nicol in view of Buch's platform/OS of its power management multiprocessing system such that it would include a task load table (process management table 23) that is dynamically updated, as taught in Matoba. The suggestion/motivation for doing so would have been to provide the predicted result of an improvement in power consumption control (see Matoba, col. 1, lines 48-57, col. 2, lines 48-52). Therefore, it would have been obvious to one of ordinary skill in the art to combine Nicol, Buch and Matoba to obtain the invention of claim 4.

25. As to claim 5, Buch (see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2) and Matoba (col. 3, lines 30-43, col. 4, lines 3-6, col. 9, lines 58-65, Fig. 1, items 11-14, 18, 23, 25, 27, 29) teaches wherein: the main processing unit includes a task allocation unit operatively

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coupled to the task load table; and the method includes using the main processing unit to re-allocate at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks.

26. As to claim 6, Buch (see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2) and Matoba (col. 8, lines 31-32, col. 9, lines 58-65) teaches further comprising re-allocating all of the tasks of a given one of the sub-processing units to another one of the sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

27. As to claim 7, Buch (see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2) and Matoba (col. 8, lines 31-32, col. 9, lines 58-65) teaches further comprising re-allocating some of the tasks of a given one of the sub-processing units to one or more of the other sub-processing units based on the associated processor loads such that the given one of the sub-processing units is not scheduled to perform any tasks.

28. As to claims 13-15 and 17, they are rejected for the same reasons as stated in the rejections of claims 4-7, respectively.

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29. As to claim 16, Buch (Fig. 5; see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2) and Nicol (Fig. 2, item 140, col. 4, lines 17-53) teach wherein the main processing unit includes a power supply controller operatively coupled to the task allocation unit and operable to issue the power-off command signal to the given one of the sub-processing units in response to an indication from the task allocation unit that the given one of the sub-processing units is not scheduled to perform any tasks.

30. As to claim 18, Buch (Fig. 5; see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2) and Nicol (Fig. 2, item 140, col. 4, lines 17-53) teach wherein the main processing unit includes a power supply controller operatively coupled to the task allocation unit and operable to issue the power-off command signal to the given one of the sub-processing units in response to an indication from the task allocation unit that the given one of the sub-processing units is not scheduled to perform any tasks.

31. As to claims 28-31, they are rejected for the same reasons as stated in the rejections of claims 4-7, respectively.

32. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (hereinafter Nicol) (US 6,141,762) in view of Buch, and further in view of Bertin et al. (hereinafter Bertin) (US 6,345,362 B1).

33. As to claim 21, Nicol in view of Buch do not expressly teach wherein at least one of the main processing unit and one or more of the sub-processing units are formed using a silicon-on-insulator fabrication process. However, Bertin teaches wherein at least one of the main processing unit and one or more of the sub-processing units are formed using a silicon-on-insulator fabrication process (col. 1, lines 43-47). One of ordinary skill in the art would have known to modify Nicol in view of Buch such that it would include the teachings of Bertin, specifically, wherein at least one of the main processing unit and one or more of the sub-processing units are formed using a silicon-on-insulator fabrication process. The suggestion/motivation for doing so would have been to provide the predicted result of allowing its circuit elements to be insulated from adjacent elements and for increasing control by being able to vary the threshold voltage (col. 1, lines 43-47).

34. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (hereinafter Nicol) (US 6,141,762) in view of Buch, and further in view of Rhee et al. (hereinafter Rhee) (US 2002/0091954 A1).

35. As to claim 23, Nicol in view of Buch is silent wherein one or more of the sub-processing units are remotely located from one another. However, Rhee also teaches a networked multiprocessing computer system that optimizes power efficiency (page 1, [0002], [0008], page 2, [0032], [0034], Fig. 1, items 12, 14, 16, 18, 20). Nicol, Buch and Rhee are analogous art

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because they are all in the same field of endeavor of multiprocessing and all attempting to solve the problem of optimizing power efficiency within its multiprocessing system. One of ordinary skill in the art would have known to modify Nicol in view of Buch's multiprocessing system such that its sub-processing units could be located remotely on a network, as taught in Rhee. The suggestion/motivation for doing so would have been to provide the predicted result of extending its power conservation abilities to portable units that are remote (see Rhee, page 1, [0006]). For portable units that operate on battery power, this would further reduce the required amount of recharging of the battery, which is a benefit and convenience to the user (see Rhee, page 1, [0007]). Therefore, it would have been obvious to one of ordinary skill in the art to combine Nicol, Buch, and Rhee to obtain the invention of claim 23.

36. Claims 34-35 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (hereinafter Nicol) (US 6,141,762) in view of Matoba (US 5,913,068).

37. As to claim 34, Nicol teaches an apparatus (see Abstract), comprising:

a plurality of sub-processing units (Fig. 2, items 101-104), each operable to perform processor tasks; and

a bus circularly interconnecting the sub-processing units such that transfers between any two sub-processing units may occur directly as between adjacent sub-processing units or through one or more intermediate sub-processing units as between more distant sub-processing units

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(clock lines interconnected between adjacent processing elements as well as non-adjacent processing elements) (Fig. 2, items 101-104, 110, col. 4, lines 38-53),

wherein a processing element (Fig. 2, item 100) is operable to: (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units (col. 2, lines 18-27, col. 5, col. 5, lines 23-28); (ii) re-allocate at least some of the tasks based on their associated processor loads (col. 2, lines 18-24).

38. As shown above, Nicol does teach having a processing element monitor and allocate/reallocate the tasks using an operating system (Fig. 2, item 100). However, Nicol is silent in having the sub-processing units (i) monitor the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and (ii) re-allocate at least some of the tasks based on their associated processor loads. However, Matoba teaches having a plurality of processors (CPU0, CPU1, CPU2, CPU3) (Fig. 1, items 11-14) interconnected by a CPU bus, which share access to a "process management table" 23, "load data of each processor" 29, "Process Management Software" 25, "Processor Load Measuring Software" 27, etc., in order to monitor processor tasks and associated processor loads that are allocated to be performed by the respective processors of CPU0, CPU1, CPU2, and CPU3 (see Fig. 1, col. 4, lines 3-6, col. 5, lines 37-39 and 61-63, col. 6, lines 15-19, col. 8, lines 31-42, col. 9, lines 58-67). Nicol and Matoba are both analogous art because they are in the same field of endeavor of multiprocessing and all attempting to solve the same problem of improving power management/conservation. One of ordinary skill in the art would have known to modify Nicol's power management multiprocessing system such that it would include having the sub-processing units (i) monitor the processor tasks and associated processor loads therefor that are allocated to

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be performed by the respective sub-processing units; and (ii) re-allocate at least some of the tasks based on their associated processor loads, as taught in Matoba's power management multiprocessing system. The suggestion/motivation for doing so would have been to provide the predicted result of power consumption control that is dynamic, more effectively performed and which allows for finer power consumption control (see Matoba, col. 1, lines 48-57, col. 2, lines 48-52, col. 9, lines 58-65). Therefore, it would have been obvious to one of ordinary skill in the art to combine Nicol and Matoba to obtain the invention of claim 34.

39. As to claim 35, Nicol teaches wherein the sub-processing units are arranged in groups and the re-allocation of one or more tasks of a sub-processing unit within a given one of the groups maintains such tasks within the given group (col. 7, lines 1-3).

40. As to claim 38, Matoba teaches wherein: the sub-processing units are operable to access a task load table containing the processor tasks and associated processor loads therefor that are allocated to be performed by the respective sub-processing units; and the sub-processing units are operable to update the task load table in response to any changes in tasks and loads (Fig. 1, items 11-14, 23, 25, 27, 29, col. 3, lines 30-43, col. 4, lines 3-6, col. 9, lines 18-19 and 58-65).

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41. Claims 36-37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (hereinafter Nicol) (US 6,141,762) in view of Matoba (US 5,913,068), and further in view of Buch.

42. As to claims 36-37, Nicol in view of Matoba is explicitly silent wherein the re-allocation of the tasks is performed such that at least one of the sub-processing units is not scheduled to perform any tasks and wherein the sub-processing units that are not scheduled to perform any tasks are operable to enter a low power consumption state.

43. However, Buch teaches a multi-processing system that dynamically adjusts processor power based on system workload. Particularly, the method and apparatus determines the minimum number of required processors based on the workload and sets a processor affinity to run on the determined minimum number of required processors. The free/non-required processors enter a low-power state (see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2). Nicol, Matoba and Buch are analogous art because they are both in the same field of endeavor of multiprocessing and both are attempting to solve the same problem of reducing power consumption. Thus, one of ordinary skill in the art would have known to modify Nicol in view of Matoba's multiprocessing system and method such that it would include the teachings/concepts of Buch's multiprocessing system, namely, having at least one of the sub-processing units not scheduled to perform any tasks because of the reallocation and specifically commanding the sub-processing unit that is not scheduled to perform any tasks into a low power consumption state. The suggestion/motivation for doing so would have been to provide the

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predicted result of having the ability to provide CPUs on demand by dynamically bringing more CPU's on-line to meet increased server workload, and vice versa (Buch - col. 4, line 63 through col. 5, lines 1-2). Furthermore, it would optimize efficiency by ensuring that only the minimum number of required processors are being used, while the unused/free processors enter into a low-power state (see Abstract).

44. As to claim 39, Matoba teaches wherein the sub-processing units are operable to re-allocate all of the tasks of a given one of the sub-processing units to another one of the sub-processing units based on the associated processor loads (Fig. 1, items 11-14, 23, 25, 27, 29, col. 3, lines 30-43, col. 4, lines 3-6, col. 9, lines 18-19 and 58-65). Nicol in view of Matoba is explicitly silent wherein re-allocating occurs when one of the sub-processing units is not scheduled to perform any tasks. However, Buch teaches a multi-processing system that dynamically adjusts processor power based on system workload. Particularly, the method and apparatus determines the minimum number of required processors based on the workload and sets a processor affinity to run on the determined minimum number of required processors. The free/non-required processors enter a low-power state (see Abstract; Fig. 3; Fig. 4; col. 4, line 63 through col. 5, lines 1-2). Nicol, Matoba and Buch are analogous art because they are both in the same field of endeavor of multiprocessing and both are attempting to solve the same problem of reducing power consumption. Thus, one of ordinary skill in the art would have known to modify Nicol in view of Matoba's multiprocessing system and method such that it would include the teachings/concepts of Buch's multiprocessing system, namely, having at least one of the sub-processing units not scheduled to perform any tasks because of the reallocation and specifically

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commanding the sub-processing unit that is not scheduled to perform any tasks into a low power consumption state. The suggestion/motivation for doing so would have been to provide the predicted result of having the ability to provide CPUs on demand by dynamically bringing more CPU's on-line to meet increased server workload, and vice versa (Buch - col. 4, line 63 through col. 5, lines 1-2). Furthermore, it would optimize efficiency by ensuring that only the minimum number of required processors are being used, while the unused/free processors enter into a low-power state (see Abstract).

Response to Arguments

45. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth Tang/
Examiner, Art Unit 2195